In the Specification:

Please amend the second paragraph on page 1, beginning at line 12 as follows:

In almost any field ~~fields~~ of modern semi-conductor technology, ~~technology~~ binary signals, or signals encoding information represented in binary form, are transmitted. The so-called single-ended signaling technique provides particularly low requirements as regards circuitry and, therefore, particularly low manufacturing costs. According to the single-ended signaling technique, an electrical signal is transmitted via a single line. A reference potential is preferably transmitted via a second single line. The voltage of the electrical signal against the reference potential encodes (in binary form) the information to be transmitted. The single-ended signaling technique, however, comprises serious disadvantages. Among these are a low signal swing, the necessity of providing an additional synchronization signal, reference voltage or reference current, and insufficient suitability for high transmission rates, or band-widths, and great cable lengths.

Please amend the third paragraph on page 5, beginning at line 25 as follows:

A device 50 includes a delay circuit or member consisting of a first partial delay member 52 and a second partial delay member 54. An input 56 of the delay member is the input of the first partial delay member 52 and is also connected to the output 34 of the transmission line 30. An output 58 of the first partial delay member 52 is connected to an input 60 of the second partial delay member 54. An output 62 of the second partial delay member 54 is also the output of the delay member. The device 50 further comprises [[a]] differential amplifier circuitry 70 having a first input (+) 72, a second input (-) 74, a strobe input (str.), or third input 76, and an output 78. The first input 72 of the differential amplifier circuitry 70 is connected to the input 56 of the delay member and to the output 34 of the transmission line 30, the second input 74 of the differential amplifier circuitry 70 is connected to the output 62 of the delay member, and the third input 76 of the differential amplifier circuitry 70 is connected to the output 58 of the first partial delay member 52 and to the input 60 of the second partial delay member 54. The output 78 of the differential amplifier circuitry 70 is also the output of the device 50.

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Please amend the fourth paragraph on page 6, beginning at line 19 as follows:

With respect to the mode of operation of the first embodiment of the present invention illustrated in FIG. 1, the following refers to FIG. 2 and 3. FIG. 2 and 3 are schematic diagrams representing the time dependencies of the signals applied to the inputs 72, 74, 76 of the differential amplifier 70. In each case, the time t is ascribed to the abscissa, and the time-dependent potentials (U), or levels, of the three signals are ascribed to the ordinate. At the very top in each of FIGS. 2 and 3, an input signal 102 applied to the input 56 of the delay member is represented, which is generated by the driver 10 and transmitted by the transmission line 30 to the input 56 of the delay member. The input signal 102 is at the same time applied to the first input 72 of the differential amplifier <u>circuitry</u> 70. Below <u>input signal 102 there</u> is represented a partially delayed signal 104, which is generated by the first partial delay member 52 from the input signal 102 and is applied to the third input 76 of the differential amplifier <u>circuitry</u> 70. Below the partially delayed signal 104 there is represented a delayed signal 106, which is generated by the second partial delay member 54 from the partially delayed signal 104 and which is applied to the second input 74 of the differential amplifier <u>circuitry</u> 70. In FIG. 2 and 3, the input signal 102, the partially delayed signal 104 and the delayed signal 106 are each represented with an arbitrary offset along the ordinate in order to avoid any overlaps. At the very bottom in FIG. 2 and 3 each, the three signals 102, 104, 106 are represented in an overlapped position and with their actual potential differences, respectively.

Please amend the third paragraph on page 7, beginning at line 21 as follows:

In the embodiment shown, the delay of the delay member corresponds to the duration of the positive part 112 and to the negative part 114 of the bipolar pulse, respectively. Accordingly, in FIG. 2, the negative part 114 of the bipolar pulse of the input signal 102 coincides, in terms of time, with the positive part 112 of the bipolar pulse in the delayed signal 106. The delay of the first partial delay member 52 and the delay of the second partial delay member 54 each amount to approximately half of the delay of the delay member. Correspondingly, the edge 116 between the positive part 112 and the negative part 114 of the bipolar pulse in the partially delayed signal 104 coincides, in terms of time, with the negative part 114 of the bipolar pulse in the input signal 102 and with the positive part 112 of the bipolar pulse in the delayed signal 106. The coincidence of the negative part 114 of the bipolar pulse in the input signal 102 applied to the first input 72 of the differential amplifier circuitry 70, of the positive part 112 of the bipolar pulse in the delayed signal 106 applied to the second input 74 of the differential amplifier circuitry 70 and of the falling edge 116 of the bipolar pulse in the partially delayed signal 104 applied to the third input 76 of the differential amplifier circuitry 70 at the time t_1 ~~t.sub.1~~ is utilized in accordance with the present invention in order to decode a logic 1 from the bipolar pulse with an especially high degree of reliability. It is clearly recognizable that the illustrated coincidence of the three described features in the three signals 102, 104, 106 enables safe decoding of the logical 1 encoded in the bipolar pulse.

Please amend the third paragraph on page 8, beginning at line 27 as follows:

In accordance with a first variation of the embodiment of the present invention illustrated in FIG. 1, the differential amplifier circuitry 70 forms a difference signal only from the input signal applied at its first input 72 and from the delayed signal applied at its second input 74, which difference signal it outputs at its output 78. A positive difference signal exceeding a predetermined positive threshold indicates that the input signal comprises a bipolar pulse, which encodes a logical 0, as represented in FIG. 3. A difference signal falling below a predetermined negative threshold indicates that a bipolar pulse is present, which encodes a logical 1, as represented in FIG. 2. The difference signal output at the output 78 of the differential amplifier circuitry 70 may be interpreted correspondingly by a downstream circuit, which is not represented in FIG. 1, in order to decode a logical 0 and a logical 1, respectively. Alternatively, differential amplifier circuitry 70 may include comparator circuit 70a, which compares the difference signal ~~is compared~~ to the predetermined positive and predetermined negative threshold already in the differential amplifier circuitry 70, and, already at its output 78, the differential amplifier 70 outputs a signal, ~~signal~~ which represents the decoded logical 0 and logical 1, respectively. The subdivision of the delay member in the partial delay members 52, 54 in addition to the third input 76 of the differential amplifier are not required with this variation and may be omitted.

Please amend the second paragraph on page 9, beginning at line 14 as follows:

In accordance with a second variation of the embodiment illustrated in FIG. 1, the differential amplifier circuitry 70 additionally detects the partially delayed signal 104 applied at its third input 76 and outputs, at its output 78, a logical 0, only if the difference signal exceeds the predetermined positive threshold and, at the same time, the partially delayed signal 104 comprises a rising edge, and outputs a logical 1, only if the difference signal falls below the predetermined negative threshold and, at the same time, the partially delayed signal 104 comprises a negative edge 116. Alternatively, the differential amplifier circuitry 70 outputs at its output 78 one or more output signals in series or in parallel, which indicate whether the difference signal exceeds the predetermined positive threshold or falls below the predetermined negative threshold and whether the partially delayed signal 104 comprises a positive or a negative edge 116.

Please amend the second paragraph on page 10, beginning at line 10 as follows:

In FIG. 4, a second embodiment of the present invention is represented, which differs from the first embodiment represented by means of FIG. 1 only in that the delay member consists of a plurality of delay members 132, . . . , 144, which are connected in series, and in that the differential amplifier <u>circuitry </u>70 comprises a plurality of first inputs 72a, . . . , 72z and a plurality of second inputs 74a, . . . , 74z. The first inputs 72a, . . . , 72z and the second inputs 74a, . . . , 74z of the differential amplifier <u>circuitry </u>70 are connected to various points, or taps, within the chain of delay members 132, . . . , 144, in order to tap different signals which are partially delayed by delay times different from each other. The differential amplifier <u>circuitry </u>70 is implemented such that, for a finite discrete amount of durations of the positive parts 112 and of the negative parts 114 or for durations of the positive parts 112 and of the negative parts 114 within one or several value intervals, it selects an adapted first input 72a, . . . , 72z and an adapted second input 74a, . . . , 74z each, such that the total delay between the signal applied to the selected first input 72a, . . . , 72z and the input applied to the selected second input 74a, . . . , 74z corresponds at least approximately to the duration of the positive part 112 and of the negative part 114 of a bipolar pulse of an input signal applied to the input 56 of the delay member. By means of an asymmetric selection of the first input 72a, . . . , 72z and of the second input 74a, . . . , 74z it can be accounted for an asymmetry of a bipolar pulse, which expresses itself in different durations of the positive part 112 and of the negative part 114. The selection of the first input 72a, . . . , 72z and of the second input 74a, . . . , 74z is effected either automatically by the differential amplifier <u>circuitry </u>70 or it is specified from outside by another device or by a person operating the device 50. Alternatively, also the strobe input, or third input, 76 of the

differential amplifier circuitry 70 is selected according to the bit rate, or to the data transmission rate, or to the duration of the positive part 112 and of the negative part 114 of the bipolar pulse.